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(54) Method for manufacturing semiconductor integrated circuit structures

(57) A method for manufacturing circuit structures integrated in a semiconductor substrate (1) that includes regions (2), in particular isolation regions, the method comprising the steps of:

- depositing a conductive layer (3) to be patterned onto said semiconductor substrate (1);
- forming a first mask (4b) of a first material on said conductive layer (3);
- forming a second mask (5b) made of a second material that is different from the first and provided with first openings (10,12) of a first size (A) having spacers (8,8a) formed on their sidewalls to uncover portions of said first mask (4b) having a second width (B) which is smaller than the first;
- partly etching away said conductive layer (3) through said first and second masks (4b,5b) such to leave grooves (13) of said second width (B);
- removing said second mask (5a) and said spacers (8); and
- etching said grooves (13) through said first mask (4b) to uncover said regions (2) provided in said substrate (1) and form conductive lines (3a).

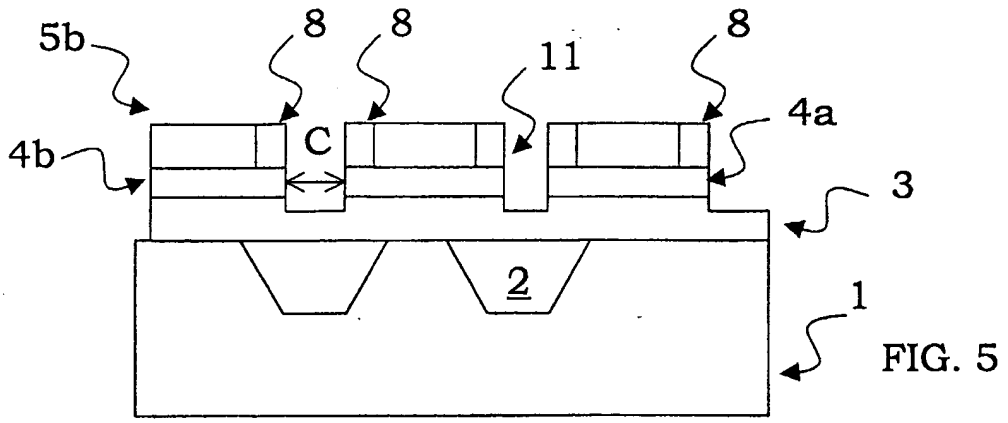

FIG. 5

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Description

Application Field

[0001] The present invention relates to a method for manufacturing circuit structures integrated in a semiconductor substrate, in particular lines of a conductive material in sub-micron circuit structures.

[0002] Specifically, the invention relates to a method for manufacturing circuit structures integrated in a semiconductor substrate, comprising isolation regions, the method comprising the steps of:

- depositing a conductive layer to be patterned onto said semiconductor substrate.

[0003] Particularly but not limited to, the invention relates to a method of forming lines of a conductive material on a semiconductor substrate, wherein the line spacing is closer than that allowed by conventional photolithography techniques and continuously variable. The following description makes reference to this application field for convenience of explanation only.

Prior Art

[0004] As it is well known, transferring patterns that have been defined in a light-sensitive layer (mask) to one or more layers beneath is a basic technical step in the integrated circuit fabricating process.

[0005] Also known is that the microelectronics industry has long been pursuing a reduction in the size of the several circuit structures that comprise an integrated circuit.

[0006] A first prior solution to the problem of bringing the spacing of structures patterned on silicon down to a value below that the one allowed by conventional photolithography techniques is based on the controlled oxidation of a silicon oxide mask, used for patterning a layer beneath.

[0007] Although this first solution is advantageous under different point of views, it presents several shortcomings. This solution comes out to be particularly crucial if structures of a conductive material, such as conductive lines, are to be formed. This because the realization of the silicon oxide mask, while effectively achieving a high mask-to-conductive material selectivity, it often harms the interfacing oxide layers as the mask is removed.

[0008] Alternately, the use of conductive or "hybrid" materials such as polysilicon, silicon nitride (Si_3N_4), silicon oxynitride (SiON), or silicide layers employed to realize the mask, guarantees the integrity of the beneath oxide layers, but it does not allow to optimize the mask-to-conductive material selectivity.

[0009] In other words, when plasma etching is used, as is conventional practice in order to pattern conductive material layers, the mask employed for layer patterning wears out too much during the etching process. On the other hand, a highly selective etch is does not assure vertical profile where the thickness of the materials exceeds limiting values.

[0010] A second prior solution to realize closely spaced lines of a conductive material provides for spacers to be formed along the lithographic mask sides for narrower gaps between the conductor material lines.

[0011] Although achieving this objective, not even this solution is devoid of shortcomings, mainly because such spacers on a photoresist mask introduce problems due to the material of the spacers that are incompatible with the light-sensitive resin.

[0012] Thus, neither of the above prior solutions are really suitable to pattern specific structures such as the floating gate regions of a flash memory, for example, where polysilicon lines need to be provided with vertical profiles on substrates in which isolation regions or thin interfacing oxide layers are realized.

[0013] The underlying technical problem of the present invention is to provide a method of forming lines of a conductive material in integrated circuits, which method has suitable structural features such to allow the lines of conductive material to be formed very closed to each other, without damaging any structures previously formed in the layers beneath, thereby to overcome the shortcomings of manufacturing methods according to the prior art.

Summary of the Invention

[0014] The solution idea at the basis of this invention is the one of using two successive masks made of different dielectric materials in order to define closely spaced lines of a conductive material. Advantageously, the method of this invention comprises forming spacers along the sidewalls of the first mask.

[0015] Based on this idea, the technical problem is solved by a method as previously indicated and as defined in the characterizing part of Claim 1.

[0016] The features and advantages of the method according to the invention should become apparent from the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

[0017] In the drawings:

- Figures 1 to 8 are schematic cross-section views of a portion of circuit integrated during different steps of the manufacturing method according to the invention; and
- Figures 9 and 10 are schematic cross-section views of a portion of a circuit integrated at different steps of a modified embodiment of the manufacturing

method according to the invention.

Detailed Description

[0018] The process steps described here below do not form a complete an integrated circuit. This invention can be implemented, along with current integrated circuit manufacturing techniques, and only such commonly used process steps necessary to understand this invention are included in the description.

[0019] The figures representing cross-sectional views taken through portions of an integrated circuit undergoing fabrication are not drawn to scale, but rather to highlight major features of the invention.

[0020] With reference to such figures, a method for manufacturing integrated circuits on a semiconductor substrate, in particular a method for forming lines of a conductive material in sub-micron circuit structures.

[0021] Shown best in Figure 1 is a semiconductor substrate 1 including an isolation region 2 that is for example oxide.

[0022] This region is provided in the semiconductor substrate 1 as shown, or is formed thereon as an insulative layer, for example.

[0023] A conductive layer 3, for example of polycrystalline silicon, a first protective layer 4, for example of silicon nitride, and a second protective layer 5, for example of oxide, are formed on the semiconductor substrate 1 in this order.

[0024] In particular according to the invention, the conductive layer 3 and second protective layer 5 are highly selective to each other, whereas the selectivity of the first protective layer 4 lies in between.

[0025] A photoresist layer 6 is then deposited onto the second protective layer 5. Using conventional lithographic techniques, the photoresist layer 6 is exposed and developed to uncover portions of the second protective layer 5 having a width A.

[0026] Lines 5a are defined by plasma etching in the second protective layer 5, which are mutually separated by first openings 10, having a width equal to the first width A. The photoresist layer 6 is then removed as shown in Figure 2.

[0027] At this stage, spacers 8 are formed inside the first openings 10.

[0028] Advantageously, these spacers 8 are formed by first depositing a third protective layer 7, e.g. of the same material as the second layer 5, having a thickness B as shown in Figure 3.

[0029] Spacers 8 of a protective material can be defined by a plasma etch. The structure comprising of the lines 5a and the spacers 8 provides a first mask 5b, wherein second openings 11 having a second width C=A-2B are defined.

[0030] By adjusting the thickness of the third protective layer 7, the width of the second openings 11 can be adjusted to far less than is allowed by conventional lithographic techniques.

[0031] The first mask 5b of this invention is then used as a screen to fully etch and remove the first protective layer 4 aligned with of the openings 11, and partly remove the conductive layer 3 to leave it formed with grooves 13, as shown in Figure 5.

[0032] Thereafter, the first mask 5b is removed by using conventional techniques like wet etching. Advantageously in this invention, the conductive layer 3 is not completely removed by the previous partial etch, so that it will be protecting the isolation regions 2 provided on the substrate 1 that otherwise would be damaged by the step of removing the first protective layer 4.

[0033] Thus, in the first protective layer 4, there are defined lines 4a at spacings of C as shown in Figure 6. The lines 4a form a second mask 4b.

[0034] By etching the conductive layer 3 through the second mask 4b, the layer 3 etching step is completed. As a result, the conductive layer 3 has a plurality of conductive lines 3a patterned thereon.

[0035] According to the invention, the second mask 4b comprises a material that is highly selective to the material of the isolation regions 2. Thus, the isolation regions 2 provided on the substrate 1 are safeguarded during the final etching of the conductive layer 3 as shown in Figure 7.

[0036] The process for defining closely spaced conductive lines 3a according to the invention is then completed with removing the first mask 4b that is selective to both the conductive layer 3 and the isolation regions 2, as shown in Figure 8.

[0037] Figures 9 and 10 illustrate a modified embodiment of the manufacturing method according to this invention.

[0038] In particular, a conductive layer 3, a first protective layer 4 and a second layer 5, in this order, are formed on the semiconductor substrate 1. The second protective layer 5 is subjected to a polymerizing plasma etching step whereby openings 12, having sloping sidewalls, are formed as shown in Figure 9.

[0039] A mask 5b is thus provided, wherein the vertical cross-section width of the opening 12 is not constant and decreases in a direction toward the first protective layer 4. Accordingly, the section of these openings 12 will pass from a first width A to a second width C, that is smaller than the first closed to the protective layer. This because the polymerizing etching step results in spacers 8a being formed within the opening 12 to provide it with flared sidewalls.

[0040] These spacers 8a are formed from the polymer material that is present in the polymerizing plasma employed to make the openings 12.

[0041] The process of this invention is then carried on through the steps previously described in relation to Figures 4 to 8, thereby producing the integrated structure shown in Figure 10.

[0042] Summarizing, the method of this invention comprises using a double mask in the manufacturing process according to the invention, comprising first and

second overlaid masks 5b and 4b that are employed to pattern a conductive layer 3 on which they have been formed. The first protective mask 5b, made from a layer of an insulating material (e.g., silicon oxide), is formed with openings 11, 12 to uncover portions of the underlying layer which are smaller than those allowed by conventional photolithographic techniques.

[0043] The first mask 5b is employed to carry out an etching step of the second mask 4b beneath and a step of partly etching the conductive layer 3. Advantageously, the second mask 4b is made from a material of intermediate selectivity in comparison with the layers 5 and 3 in which it is formed.

[0044] The first mask 5b is then removed. The isolation regions 2 are undamaged by the removal of the first mask 5b because they are protected by the layer 3 of conductive material having only been removed in part by the previous etching step.

[0045] The second mask 4b is subsequently employed to just etch away the conductive layer 3 left over.

[0046] Advantageously, the thickness of the remaining conductive layer 3 can be controlled as desired such that a etch of high mask-to-layer selectivity will have no effect on the vertical opening profiles in the layer 3 of conductive material.

[0047] The above-described method suits especially the patterning of gate structures of a memory or transistors to provide a dimension pitch that is smaller than that defined by conventional photolithographic techniques. By using a double mask of an insulating material, in particular a dielectric material, a relatively simple and controllable process can be developed in order to define sub-lithographic pitches which will safeguard isolation structures previously formed in the wafer, such as interfacing oxides, isolation regions of the LOCOS and STI types, or any being defined.

Claims

1. A method for manufacturing circuit structures integrated in a semiconductor substrate (1) that includes regions (2), in particular isolation regions, the method comprising the steps of:

   - depositing a conductive layer (3) to be patterned onto said semiconductor substrate (1);
   - **characterized in that** it further comprises the following steps:
   - forming a first mask (4b) of a first material on said conductive layer (3);
   - forming a second mask (5b) made of a second material that is different from the first and provided with first openings (10,12) of a first width (A) having spacers (8,8a) formed on their sidewalls to uncover portions of said first mask (4b) having a second width (B) which is smaller than the first;
   - partly etching away said conductive layer (3) through said first and second masks (4b,5b) such to form grooves (13) of said second width (B);
   - removing said second mask (5a) and said spacers (8); and
   - etching said grooves (13) through said first mask (4b) to uncover said regions (2) provided in said substrate (1) and form conductive lines (3a).

2. A method for manufacturing circuit structures according to Claim 1, **characterized in that** said first and second masks (4b,5b) respectively are made of first and second protective layers (4,5).

3. A method for manufacturing circuit structures according to Claim 2, **characterized in that** said first and second protective layers (4,5) are made out of highly selective materials in comparison with said conductive layer (3).

4. A method for manufacturing circuit structures according to Claim 2, **characterized in that** said first and second protective layers (4,5) are selective materials to each other.

5. A method for manufacturing circuit structures according to Claim 2, **characterized in that** said first and second protective layers (4,5) are dielectric layers.

6. A method for manufacturing circuit structures according to Claim 5, **characterized in that** said first protective layer (4) is a layer of silicon nitride.

7. A method for manufacturing circuit structures according to Claim 5, **characterized in that** said second protective layer (5) is a layer of silicon oxide.

8. A method for manufacturing circuit structures according to Claim 2, **characterized in that** said spacers (8) are formed by the following steps:

   - depositing a third protective layer (7) onto said second mask (5b) after said openings (10) are formed; and
   - removing said third protective layer (7) to uncover portions of said first mask (4b) having a second width (B) smaller than the first.

9. A method for manufacturing circuit structures according to Claim 1, **characterized in that** said spacers (8) are obtained by polymerizing plasma etching through said second mask (5b).

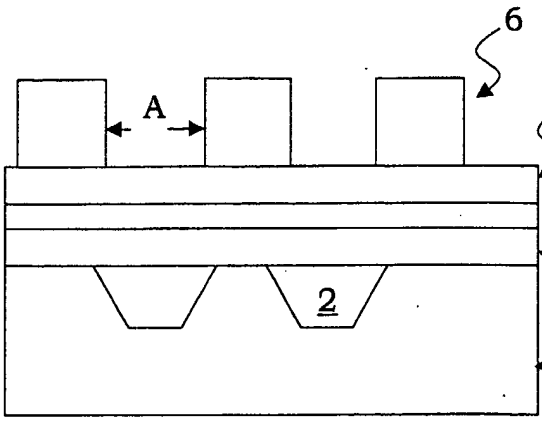

FIG. 1

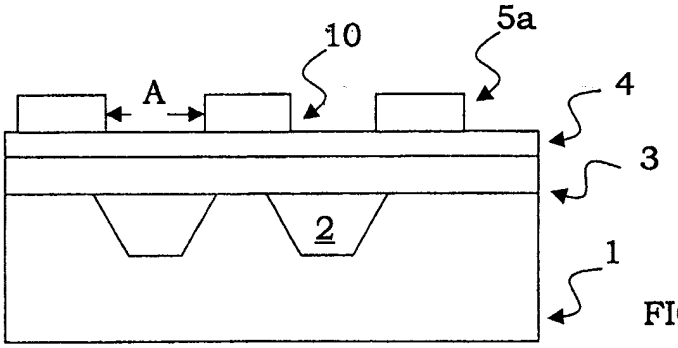

FIG. 2

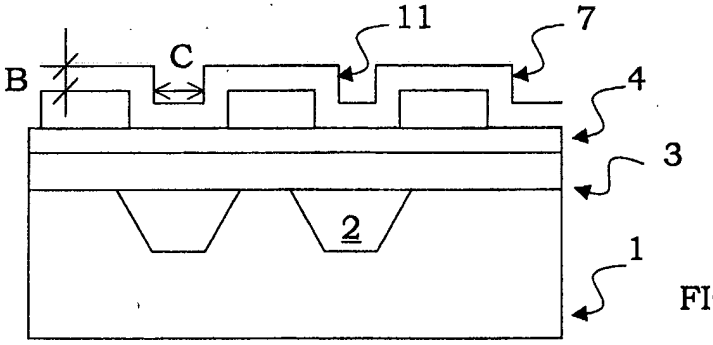

FIG. 3

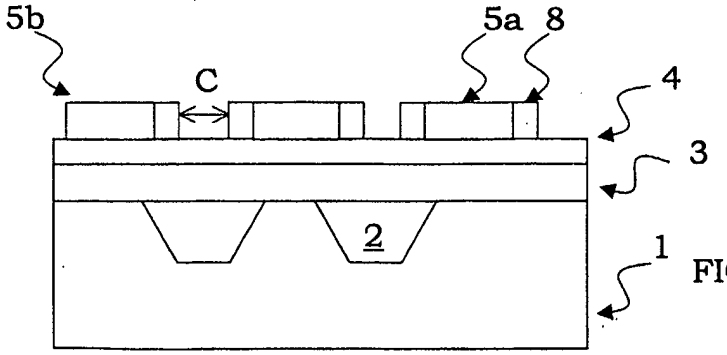

FIG. 4

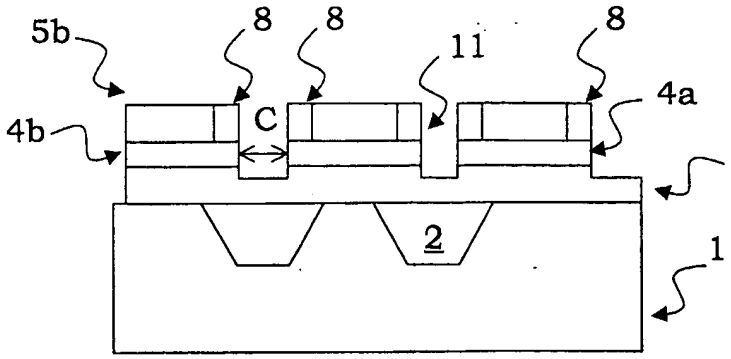

FIG. 5

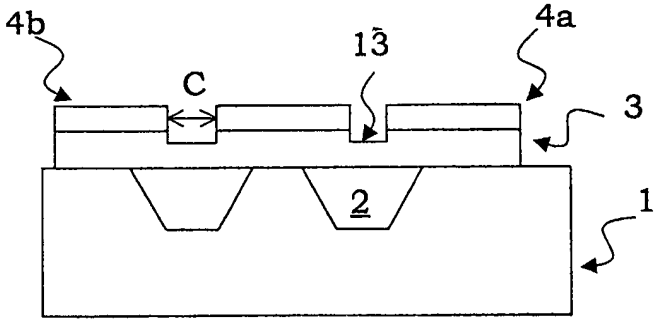

FIG. 6

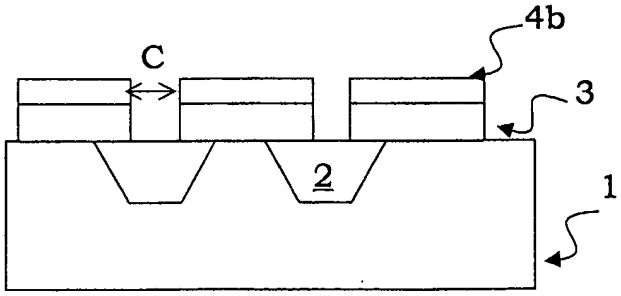

FIG. 7

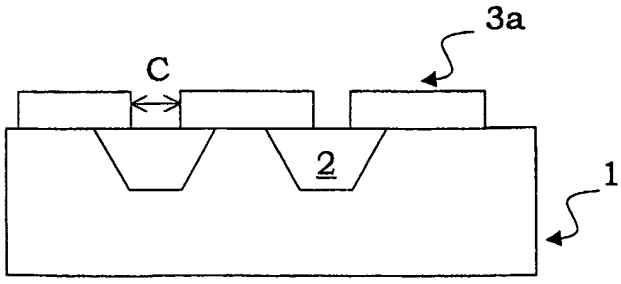

FIG. 8

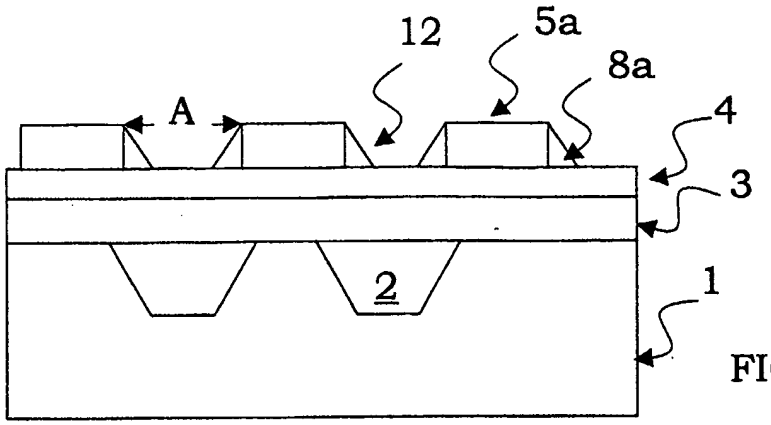

FIG. 9

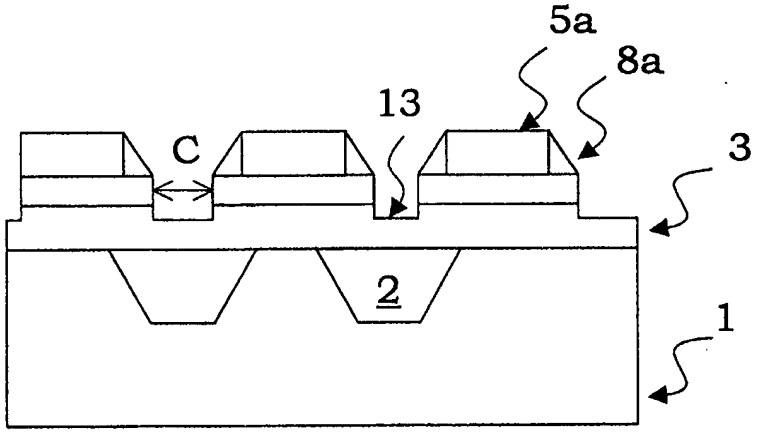

FIG. 10

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EUROPEAN SEARCH REPORT

Application Number
EP 02 42 5505

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 2001/041309 A1 (KIM NAM-HUN ET AL) 15 November 2001 (2001-11-15) * figures 2,3 * ---	1-9	H01L21/3213 H01L21/033
A	US 6 242 795 B1 (CHANG MING-LUN) 5 June 2001 (2001-06-05) * figures 3A-3F * ---	1-9	
A	US 5 893 748 A (LIN MING-REN) 13 April 1999 (1999-04-13) * figures 8,9 * -----	1-9	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	17 February 2003	Le Meur, M-A

CATEGORY OF CITED DOCUMENTS

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